IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Patent Application

Appellants(s):	Dohmen et al.
Case:	9-1-4-9
Serial No.:	09/976,729
Filing Date:	October 12, 2001
Group:	2133
Examiner:	Joseph D. Torres

I hereby certify that this paper is being deposited on this date with the U.S. Postal Service as first class mail addressed to the Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450

Signature: Tina Maurer Date: October 22, 2004

Title: High Speed Syndrome-Based FEC Encoder and Decoder and System Using Same

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APPEAL BRIEF

Mail Stop Appeal Brief - Patents
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Sir:

Appellants hereby appeal the final rejection dated May 10, 2004, of claims 1-14, 19, and 25 of the above-identified patent application.

REAL PARTY IN INTEREST

The present application is assigned to the Agere Systems Inc., as evidenced by an assignment recorded on January 10, 2002 in the United States Patent and Trademark Office at Reel 012490, Frame 0693. The assignee, Agere Systems Inc., is the real party in interest.

RELATED APPEALS AND INTERFERENCES

There are no related appeals or interferences.

STATUS OF CLAIMS

Claims 1-14, 19, and 25 are pending in the above-identified patent application. Claims 1-3 and 25 remain rejected under 35 USC §102(e) as being anticipated by Chen (U.S. Patent No. 6,571,368), claims 4 and 6 remain rejected under 35

USC §103(a) as being unpatentable over Chen in view of Yun (U.S. Patent No. 5,526,368), claims 8, 9, and 19 remain rejected under 35 USC §103(a) as being unpatentable over Chen in view of White (U.S. Patent No. 5,754,563), and claims 10-14 remain rejected under 35 USC §103(a) as being unpatentable over Chen in view of Mastrovito, VLSI designs for multiplication over finite fields *GF(2^m^)*," Int'l Conf. on Applied Algebra, Algebraic Algorithms, and Error-Correcting Codes, 297-309, Rome, (1988). The Examiner indicated that claims 5 and 7 would be allowable if rewritten in independent form including all of the limitations of the base claims and any intervening claims.

STATUS OF AMENDMENTS

There have been no amendments to the claims filed subsequent to the final rejection. The specification was amended to correct typographical errors.

SUMMARY OF INVENTION

The present invention is directed to a decoder, encoder and corresponding system for providing fast Forward Error Correcting (FEC) decoding and encoding of syndrome-based error correcting codes (page 5, line 26, to page 13, line 10). Three-parallel processing is performed by elements of the system. More particularly, in an illustrative embodiment, a decoder performs three-parallel syndrome generation and error determination and calculations, and an encoder performs three-parallel encoding (page 13, line 12, to page 20, line 6). Low power and complexity techniques are used to save cost and power yet provide relatively high speed encoding and decoding (page 20, line 7, to page 26, line 22).

ISSUES PRESENTED FOR REVIEW

i. Whether claims 1-3 and 25 are properly rejected under 35 USC §102(e) as being anticipated by Chen;

ii. Whether claims 4 and 6 are properly rejected under 35 USC §103(a) as being unpatentable over Chen in view of Yun;

iii. Whether claims 8, 9, and 19 are properly rejected under 35 USC §103(a) as being unpatentable over Chen in view of White; and

iv. Whether claims 10-14 are properly rejected under 35 USC §103(a) as being unpatentable over Chen in view of Mastrovito.

GROUPING OF CLAIMS

The rejected claims do not stand and fall together. More particularly, for the reasons given below, Appellants believe that each of the dependent claims 4, 8, and 10 provide independent bases for patentability apart from the rejected independent claims.

ARGUMENT

Rejection of Claims 1 under 35 USC §102(e)

In the outstanding final Office Action, the Examiner rejected claim 1 under 35 USC §102(e) as being anticipated by Chen. The Examiner basically asserted that all limitations in claim 1 are taught by Chen.

Appellants respectfully traverse this rejection. Independent claim 1 includes the following limitations (emphases added): (1) "a plurality of key equation determination devices, each key equation determination device coupled to at least one of the N-parallel syndrome generators and being adapted to determine at least one error polynomial by using a corresponding plurality of syndromes from the at least one N-parallel syndrome generator," and (2) "a plurality of N-parallel error determination and correcting devices, one for each of the N-parallel syndrome generators, each N-parallel error correction and determination device coupled to one of the key equation determination devices and being adapted to use the at least one error polynomial produced by the one key equation determination device to correct errors in the parallel data stream."

In limitation (1), Appellants therefore claim a plurality of key equation determination devices, where each key equation determination device is adapted to determine at least one error polynomial. The only device in FIG. 6 of Chen that may be considered, for sake of argument, to determine "at least one error polynomial" is an E

array disclosed in FIG. 6 of Chen. For instance, Chen states that a second stage of a structure shown in FIG. 6 of Chen performs Euclid's algorithm. The E array includes cells 610-615, 620-625, and 630-635. Chen at col. 9, lines 9-13. Chen also states that Euclid's algorithm determines an error location polynomial $\Lambda(x)$ and an error evaluator polynomial $\Omega(x)$. Chen at col. 8, lines 54-59. Furthermore, Chen states that the error location and evaluator polynomials accumulate in the G row of the second cells 620-625 of the E array and that the polynomials pass in parallel from G row cells 620 to 625 to the cells 640 to 645 of the error evaluator array Ω_Λ. Chen at col. 9, lines 38-41.

As Chen indicates that the <u>single</u> E array in FIG. 6 of Chen is the device that determines error location and evaluator polynomials, then Chen does not disclose a <u>plurality</u> of key equation determination devices, where <u>each</u> key equation determination device is adapted to determine at least one error polynomial, as claimed in limitation (1) of independent claim 1.

Furthermore, in limitation (2) of independent claim 1, Appellants claim a plurality of N-parallel error determination and correcting devices, where each N-parallel error correction and determination device is adapted to use the at least one error polynomial produced by a corresponding key equation determination device to <u>correct</u> errors in the parallel data stream. Chen states that error location and value evaluation are performed by the error evaluator array Ω_Λ, which has cells 640-645. Chen at col. 9, lines 27-32. Chen also states that the error location polynomial and the error evaluator polynomial are evaluated to get the error locations and values, then the errors are corrected "by subtracting E(x) from the received codes." Chen at col. 6, lines 64-67. There is no indication in Chen that the error evaluator array Ω_Λ in Chen corrects errors.

Appellants can find only one disclosed device in Chen that corrects errors, and that is the Galois Field adder 516 in Chen. For instance, FIG. 26 in Chen shows control logic for the evaluation computation, but the control logic in FIG. 26 ends with sequential outputting of the error polynomial E(x). Chen at col. 17, line 47 to col. 18, line 3. Chen states that an additional step of subtracting E(x) from the received codes is

necessary, and the only device that does this subtraction in Chen is the single Galois Field adder 516 in Chen. See FIG. 5 of Chen and col. 6, lines 62-67 of Chen.

Therefore, Chen does not disclose a plurality of N-parallel error correction and determination devices, where each N-parallel error correction and determination device is adapted to use the at least one error polynomial produced by the one key equation determination device to correct errors in the parallel data stream, as claimed in limitation (2) of independent claim 1. Because Chen does not disclose at least limitations (1) and (2) of independent claim 1, independent claim 1 is patentable over Chen.

In the final Office Action, the Examiner makes an argument that one could group certain elements of FIG. 6 of Chen and groups of elements would then equate with limitations of independent claim 1. For example, the Examiner states (see paragraph spanning pages 9 and 10 of the outstanding final Office Action) that "Chen teaches a decoder comprising: a plurality of N-parallel syndrome generators (in Figure 6 of Chen, the Syndrome Generators S_0-S_{2t} can be grouped in twos [S_1,S_2], [S_3,S_4]...[S_{2t-1},S_{2t}] whereby each of the [S_{2k-1},S_{2k}], as k ranges from 1 to t, is an N=2-parallel syndrome generator; hence Chen teaches t N-2-parallel syndrome generators)."

However, there is no indication in Chen that Chen's elements can be grouped as suggested by the Examiner. Furthermore, Appellants respectfully submit that the Examiner's argument goes against the teaching of Chen. The Examiner asserts that groups of elements, such as groups of certain cells 610-615, 620-625, and 630-635 of the E array and certain cells 640-645 of the error evaluator array Ω_Λ, are equivalent to "a plurality of N-parallel error correction and determination devices," as recited in limitation (2) of independent claim 1. However, limitation (2) also generally recites that each N-parallel error correction and determination device is adapted to use the at least one error polynomial produced by the one key equation determination device to correct errors in the parallel data stream. As stated above, Appellants can find only one disclosed device in Chen that corrects errors, and that is the Galois Field adder 516 in Chen.

Therefore, Appellants respectfully submit that independent claim 1 is patentable over Chen.

Rejection of Claims 19 under 35 USC §103(a)

The Examiner rejected claim 19 under 35 USC §103(a) as being unpatentable over Chen in view of White.

In independent claim 19, Appellants claim the limitations of (A) "performing, in parallel and by using each of the plurality of syndromes generated by each of the plurality of N-parallel syndrome generations, a plurality of N-parallel decodings of the parallel data stream to determine, in parallel, a plurality of error value and error locator polynomials" and (B) "correcting errors, by using a plurality of N-parallel correction and determination processes that use the error value and error locator polynomials, in the parallel data stream." Thus, in limitation (A), a plurality of error value and error locator polynomials are determined. In limitation (B), errors are corrected by using the error value and error locator polynomials.

As described above, Chen discloses that the E array produces an error location polynomial and an evaluator polynomial. See Chen at col. 9, lines 38-41, col. 9, lines 9-13, and col. 8, lines 53-65. In independent claim 19, a plurality of error value and error locator polynomials are determined in limitation (A) and errors are corrected by using the error value and error locator polynomials in limitation (B). Thus, Chen does not disclose at least limitations (A) and (B) of independent claim 19.

Appellants respectfully submit that White does not teach or imply limitations (A) or (B) as recited in independent claim 19. In particular, White states that "[t]he output of the key equation solver is an error locator polynomial, L(x), and an error evaluator polynomial, V(x), multiplied by the constant polynomial x, i.e. xV(x)" at col. 3, lines 53-54. There is no disclosure or implication in White of determination of a plurality of error value and error locator polynomials or of correcting errors by using the error value and error locator polynomials, as claimed in limitations (A) and (B) of independent claim 19.

Because neither Chen nor White teach a plurality of error value and error locator polynomials or of correcting errors by using the error value and error locator polynomials, as claimed in limitations (A) and (B) of independent claim 19, the combination of Chen and White cannot teach these limitations.

Consequently, Appellants respectfully submit that amended claim 19 is patentable over Chen and White in combination and respectfully request the withdrawal of the §103(a) rejection of claim 19.

Conclusion

The rejections of the independent claims under §102 and §103 in view of Chen, Yun, White, and Mastrovito, alone or in any combination, are therefore believed to be improper and should be withdrawn.

Dependent Claims

Claims 4, 8, and 10 specify a number of limitations providing additional bases for patentability. Specifically, the Examiner rejected claim 4 under 35 USC §103(a) as being unpatentable over Chen in view of Yun, rejected claim 8 under 35 USC §103(a) as being unpatentable over Chen in view of White, and rejected claim 10 under 35 USC §103(a) as being unpatentable over Chen in view of Mastrovito. Claim 4 requires wherein each symbol is a symbol from one of a plurality codewords from a frame, and wherein the decoder further comprises a device adapted to determine if a codeword is uncorrectable and adapted to output a number of uncorrectable codewords in the frame. Claim 8 requires the decoder further comprises a device adapted to output a second parallel data stream comprising corrected symbols; and the decoder further comprises a device adapted to output a parallel stream of correction values, each bit in the parallel stream of correction values indicating a position in the second parallel data stream at which an error occurs. Claim 10 requires wherein each key equation determination device further comprises a plurality of multiplication circuits, each of the plurality of multiplication circuits comprising a Mastrovito standard-basis multiplier.

Regarding claim 4, the Examiner acknowledges that Chen does not disclose the use of a method for determining the number of codewords with uncorrectable errors, but asserts that Yun teaches this limitation for use in an error correcting decision process (col. 10, lines 48-51).

In the text cited by the Examiner, Yun discloses "determining whether a total number of said decoded successive codewords in which the uncorrectable error

occurs is greater than a second predetermined number." Yun does not disclose or suggest, however, that the device is *adapted to output a number of uncorrectable codewords in the frame*.

Thus, Chen and Yun, alone or in combination, do not disclose or suggest wherein each symbol is a symbol from one of a plurality codewords from a frame, and wherein the decoder further comprises a device adapted to determine if a codeword is uncorrectable and adapted to output a number of uncorrectable codewords in the frame, as required by claim 4.

Regarding claim 8, the Examiner acknowledges that Chen does not explicitly teach the specific use of the parallel correction of data, but asserts that White teaches the use of implementing a Most Likely Code Word Generator 308 (FIGS. 3, 7, and 7-A) which takes data from Error Correction Circuitry 511-515 as taught in the Chen patent in parallel whereby c(x) is a parallel data stream comprising corrected symbols and e(x) is a parallel stream of correction values, each bit in the parallel stream of correction values indicating a position in the second parallel data stream at which an error occurs.

Appellants note that White discloses that Most Likely Code Word Generator 308 determines the most-likely code word/polynomial, c(x), given the most-likely error word/polynomial and a delayed version of the received word/polynial, Δr(x). (Col. 8, lines 33-40.) White does not disclose or suggest that the decoder further comprises a device adapted to output *a parallel stream of correction values, each bit in the parallel stream of correction values indicating a position in the second parallel data stream at which an error occurs*.

Thus, Chen and White, alone or in combination, do not disclose or suggest the decoder further comprises a device adapted to output a second parallel data stream comprising corrected symbols; and the decoder further comprises a device adapted to output a parallel stream of correction values, each bit in the parallel stream of correction values indicating a position in the second parallel data stream at which an error occurs, as required by claim 8.

Regarding claim 10, the Examiner acknowledges that Chen does not explicitly teach the specific use of a Mastrovito standard-basis multiplier, but asserts that Appellants admit in the specification (page 28, lines 10-15) that the Mastrovito standard-

basis multiplier is a composite-basis multiplier over finite fields GF(2^m) with reduced complexity and higher speed (page 31, lines 16-18).

Appellants maintain that a person of ordinary skill in the art would not recognize the reduced complexity and higher speed derived from the use of Mastrovito standard-basis multipliers that was disclosed in the present disclosure (page 29, line 4, to page 31, line 18). Thus, a person of ordinary skill in the art would not look to combine Chen and Mastrovito.

Thus, Chen and Mastrovito, alone or in combination, do not disclose or suggest wherein each key equation determination device further comprises a plurality of multiplication circuits, each of the plurality of multiplication circuits comprising a Mastrovito standard-basis multiplier, as required by claim 10.

The remaining rejected dependent claims are believed allowable for at least the reasons identified above with respect to the independent claims.

The attention of the Examiner and the Appeal Board to this matter is appreciated.

Respectfully,

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APPENDIX

1. A decoder comprising:

a plurality of N-parallel syndrome generators, each of the N-parallel syndrome generators coupled to a parallel data stream and being adapted to perform a calculation each cycle with N symbols from the parallel data stream, each N-parallel syndrome generator adapted to determine, after a predetermined number of cycles, a plurality of syndromes;

a plurality of key equation determination devices, each key equation determination device coupled to at least one of the N-parallel syndrome generators and being adapted to determine at least one error polynomial by using a corresponding plurality of syndromes from the at least one N-parallel syndrome generator; and

a plurality of N-parallel error determination and correcting devices, one for each of the N-parallel syndrome generators, each N-parallel error correction and determination device coupled to one of the key equation determination devices and being adapted to use the at least one error polynomial produced by the one key equation determination device to correct errors in the parallel data stream.

2. The decoder of claim 1, wherein N is three.

3. The decoder of claim 1, further comprising a device adapted to convert a serial input data stream into the parallel data stream.

4. The decoder of claim 1, wherein each symbol is a symbol from one of a plurality codewords from a frame, and wherein the decoder further comprises a device adapted to determine if a codeword is uncorrectable and adapted to output a number of uncorrectable codewords in the frame.

5. The decoder of claim 3, wherein:

the device creates a parallel data stream having a width of 48 symbols, wherein the device outputs 48 symbols every clock cycle;

N is three;

there are 16 three-parallel syndrome generators, four key equation determination devices, and 16 three-parallel error determination and detection devices, wherein each four of the three-parallel syndrome generators and three-parallel error determination and detection devices share one of the four key equation determination devices; and

the decoder outputs a second parallel data stream having a width of 48 symbols, wherein the decoder outputs 48 symbols per clock cycle.

6. The decoder of claim 1, wherein each symbol is a symbol from one of a plurality codewords in a frame, and wherein the decoder further comprises a device adapted to output a number of corrected bit errors per frame.

7. The decoder of claim 6, wherein the decoder further comprises a device adapted to disable error correction of the decoder when the number of corrected bit errors for each of a predetermined number of frames is less than a first predetermined value and adapted to disable the decoder when a deployed forward error correcting code cannot be processed by the decoder.

8. The decoder of claim 1, wherein:

each symbol is a symbol from one of a plurality of codewords;

the decoder further comprises a device adapted to output a second parallel data stream comprising corrected symbols; and

the decoder further comprises a device adapted to output a parallel stream of correction values, each bit in the parallel stream of correction values indicating a position in the second parallel data stream at which an error occurs.

9. The decoder of claim 8, further comprising a peripheral, the peripheral performing error analyses using the parallel stream of correction values.

10. The decoder of claim 1, wherein each key equation determination device further comprises a plurality of multiplication circuits, each of the plurality of multiplication circuits comprising a Mastrovito standard-basis multiplier.

11. The decoder of claim 10, wherein each Mastrovito standard-basis multiplier has a computation delay of (one DAND + five DXOR), where DAND denotes a delay of one AND gate and DXOR denotes a delay of one XOR gate.

12. The decoder of claim 10, wherein each N-parallel error determination and correcting device further comprises a division circuit, each division circuit comprising a composite-basis divider.

13. The decoder of claim 12, wherein each composite basis divider has a computation delay of (three DAND + nine DXOR), where DAND denotes a delay of one AND gate and DXOR denotes a delay of one XOR gate.

14. The decoder of claim 13, wherein each composite basis divider further comprises an inverter having a delay of (one DAND + three DXOR).

15.-18. (Withdrawn)

19. A method comprising the steps of:

converting a serial input data stream into a parallel data stream;

performing a plurality of N-parallel syndrome generations using the parallel data stream, each of the N-parallel syndrome generations determining, after a predetermined number of cycles, a plurality of syndromes;

performing, in parallel and by using each of the plurality of syndromes generated by each of the plurality of N-parallel syndrome generations, a plurality of N-parallel decodings of the parallel data stream to determine, in parallel, a plurality of error value and error locator polynomials;

correcting errors, by using a plurality of N-parallel correction and determination processes that use the error value and error locator polynomials, in the parallel data stream; and

outputting a second parallel data stream comprising a corrected version of the parallel data stream.

20.-24. (Withdrawn)

25. The decoder of claim 1, wherein:

the parallel data stream comprises a plurality of codewords; and

the decoder is adapted to route N symbols of a given codeword to a given N-parallel syndrome generator.